

AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A circuit comprising:

a supply voltage current mirror configured to be coupled to a supply voltage source, and comprising a current output configured to be coupled to a node; the node coupling a fanout current mirror and a first programmable current mirror, the first programmable mirror having a first transistor having a first channel length modulation factor λ_1 ; and

a second programmable current mirror coupled to the supply voltage current mirror and comprising a second transistor having a second channel length modulation factor λ_2 , the second channel length modulation factor λ_2 is being larger than the first channel length modulation factor λ_1 , the second programmable current mirror being configured ~~cooperating~~ to maintain, with the first programmable current mirror, a bias current through the fanout current mirror substantially independent of voltage changes in the supply voltage source.

2. (Previously Presented) The circuit of claim 1 wherein the first programmable current mirror comprises a parallel array of programmable transistors for defining a predetermined range of current.

3. (Previously Presented) The circuit of claim 1 wherein the circuit is formed on a single integrated circuit device.

4. (Previously Presented) The circuit of claim 3 wherein the circuit is formed using complementary metal-oxide-semiconductor technology.

5. (Previously Presented) A circuit comprising:
a means for detecting changes in the voltage from a supply voltage source, the means for detecting changes comprising a means for generating a compensation signal representative of voltage changes in the supply voltage source; and
a means for generating a compensation current for application to a current mirror in response to the compensation signal.

Claims 6 and 7 (Cancelled)

8. (Previously Presented) A method for compensating for supply-voltage-induced changes to a desired current through a fanout current mirror, the method comprising:
detecting changes in the voltage from a supply voltage source;
generating a compensation current to a current path node, the compensation current representative of the voltage changes in the supply voltage source, the compensation current based on the channel length modulation factor λ_2 of a second programmable current source; and
sinking current from the current path node with a first programmable current source having a first channel length modulation factor λ_1 , λ_1 being less than λ_2 , wherein the level of

current sunk corresponds to the difference between the compensation current and the desired current through the fanout current mirror.

Claims 9 to 12 (Cancelled)

Claim 13 (Previously Presented) A circuit, comprising:

a current mirror circuit, the current mirror circuit comprising:

a first programmable current mirror and a fanout current mirror coupled to the first programmable current mirror by a node, the first programmable current mirror comprising a first transistor having a first channel length modulation factor λ_1 , the fanout current mirror coupled to a supply voltage source, and

a current compensation circuit; the current compensation circuit comprising:

a supply voltage current mirror coupled to the supply voltage source and comprising a current output coupled to the node; and

a second programmable current mirror coupled to the supply voltage current mirror comprising a second transistor with a second channel length modulation factor λ_2 , the second channel length modulation factor λ_2 being larger than the first channel length modulation factor λ_1 , the first programmable current mirror and the second programmable current mirror cooperating to maintain a bias current through the fanout current mirror substantially independent of voltage changes in the supply voltage source.

Claim 14 (Previously Presented) The circuit of claim 13 wherein the first programmable current mirror comprises a parallel array of programmable transistors for defining a predetermined range of current.

Claim 15 (Previously Presented) The circuit of claim 13 wherein the second programmable current mirror comprises a parallel array of programmable transistors for defining a predetermined range of current.

Claim 16 (Previously Presented) The circuit of claim 13 wherein the circuit is formed on a single integrated circuit device.

Claim 17 (Previously Presented) The circuit according to claim 13 wherein the circuit is formed using a complementary metal-oxide-semiconductor.